REMARKS

Claims 25-37, 39-41 are pending in the present application. Claims 25-41 were presented for examination. Claim 38 has been cancelled by amendment.

In the office action mailed July 14, 2005 (the "Office Action"), the Examiner rejected claim 29 under 35 U.S.C. 112, second paragraph, and further rejected claims 25-32 and 37-41 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,027,982 to Peidous *et al.* (the "Peidous patent"). Claims 33-36 were allowed by the Examiner.

With respect to the Examiner's rejection of claim 29 under 35 U.S.C. 112, second paragraph, claim 29 has been amended to recite that the semiconductor structure further comprises a layer of insulating material formed after removal of the mask layer that fills the trench. Claim 29 now clearly recites that the mask layer is not present when the layer of insulating material fills the trench. Consequently, the rejection of claim 29 under 35 U.S.C. 112, second paragraph should now be withdrawn.

As previously mentioned, claims 25-32 and 37-41 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Peidous patent. Claim 38 has been cancelled and the Examiner's rejection of claim 38 is now moot. Claims 25, 30, and 37 are patentably distinct from the Peidous patent because the Peidous patent fails to disclose the combination of limitations recited by the respective claims.

For example, with respect to claim 25, the Peidous patent fails to disclose a semiconductor structure including a first layer of a first material formed over a substrate and having a tapered opening therethrough over a trench formed in the substrate. The tapered opening has a first dimension on a first side adjacent the trench less than a second dimension on a second opposite side of the first layer. The semiconductor structure further includes a mask layer formed over the first layer. The mask layer has an opening therethrough with a dimension less than the second dimension of the tapered opening of the first layer. As shown in Figures 4 and 5 of the Peidous patent, the formation of the trench 35 and opening through the thin oxide layer 34, silicon nitride layer 33 and pad oxide 32 are formed in one etch step. The resulting opening through the silicon nitride layer 33 has a dimension adjacent the thin oxide layer 34 that is less than the dimension of the opening through the thin oxide layer 34. *See* Figure 4. An isotropic etch step is used to etch back the silicon nitride layer 33 to under cut the thin oxide

layer 34 and back away from the opening of the trench 35. *See* Figure 5. The resulting opening through the silicon nitride layer 33 does not have a tapered profile where the dimensions adjacent the trench are less than dimensions on a second opposite side of the layer. For the foregoing reasons, claim 25 is patentably distinct from the Peidous patent.

With respect to claim 30, the Peidous patent fails to disclose a semiconductor structure having a trench formed in a substrate where the trench has sidewalls at a first angle relative to a surface of the substrate and has a trench opening dimension. The semiconductor structure further includes a first layer of a silicon nitride material formed over the substrate and having an opening therethrough over the trench. The opening through the first layer has a dimension adjacent the trench approximately equal to the trench opening dimension and further having sidewalls at a second angle relative to the surface of the substrate that is unequal to the first angle. As previously discussed, the trench 35 and the openings through the thin oxide layer 34, the silicon nitride layer 33, and the pad oxide 32 are formed in one etch step. The resulting trench 35 and opening through the silicon nitride layer 33 have the same sidewall profile, as shown in Figure 4. That is, the angle of the sidewalls of the opening through the silicon nitride layer 33 relative of the surface of the substrate 31 and the angle sidewalls of the trench 35 relative of the surface of the substrate 31 are the same. Upon etch back of the silicon nitride layer 33, the dimension of the opening does not have a dimension adjacent to the trench 35 approximately equal to the trench opening dimension at the surface of the substrate. The etch back step for the silicon nitride layer 33 pulls the layer back away from the opening of the trench to create an area 36. For the foregoing reasons, claim 30 is patentably distinct from the Peidous patent.

With respect to claim 37, the Peidous patent fails to disclose a semiconductor structure having a trench formed in a substrate where the trench has an opening with a trench opening dimension. The semiconductor structure further includes a mask layer having an opening therethrough and located over the trench. The opening in the mask layer has a mask layer opening dimension. The structure further includes a first layer interposed between the substrate and the mask layer. The first layer has an opening undercutting the opening of the mask layer. The opening in the first layer has a dimension adjacent the mask layer greater than a dimension adjacent the substrate and greater than the mask layer opening dimension. As shown

in Figures 4 and 5, when the silicon nitride layer 33 is initially etched during the formation of the trench 35 (Figure 4) and then etched back to create the area 36 (Figure 5), the dimensions of the resulting openings through the silicon nitride layer 33 do not have a dimension adjacent the thin oxide layer 34 greater than a dimension adjacent the substrate 31 and also greater than the opening through the thin oxide layer 34. For the foregoing reasons, claim 37 is patentably distinct from the Peidous patent.

Claims 26-29, which depend from claim 25, claims 31 and 32, which depend from claim 30, and claims 39-41, which depend from claim 37, are also patentably distinct from the Peidous patent because of their dependency from a respective allowable base claim. Therefore, the rejection of claims 25-32, 37, and 39-41 under 35 U.S.C. 102(b) should now be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

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